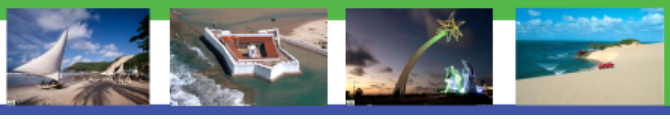
IEEE COMPUTER SOCIETY ANNUAL SYMPOSIUM ON VLSI

ISVLSI 2013

August 5-7, 2013
Natal, BRAZIL



Monday, August 5		
09:00-09:30	Opening Session	
09:30-10:30	**Keynote 1: Manuel D'Abreu (Sandisk)** **NAND Flash Memory: the Driving Technology in Digital Storage - Overview and Challenges**	
10:30-10:45	**Coffee break**	
10:45-12:25	S1: Network-on-Chip Design **Do We Need Wide Flits in Networks-On-Chip?** Junghee Lee, Chrysostomos Nicopoulos, Sung Joo Park, Madhavan Swaminathan and Jongman Kim **Determining the Test Sources/Sinks for NoC TAMs** Alexandre Amory, Edson Moreno, Marcelo Lubaszewski and Fernando Moraes **A Dependable and Power-Efficient NoC Architecture** Majed Valadbeigi, Farshad Safaei, Armin Belghadr and Bahareh Pourshirazi **Real-Time Low-Power Task Mapping in Networks-on-Chip** M. Norazizi Sham Mohd Sayuti and Leandro Soares Indrusiak	S2: Verification & Debug **Effective Combination of Algebraic Techniques and Decision Diagrams to Formally Verify Large Arithmetic Circuits** Farimah Farahmandi, Bijan Alizadeh and Zain Navabi **Mutation-based Technique for Automatic Correction of Functional Bugs in Digital Designs** Payman Behnam, Bijan Alizadeh and Zainalabedin Navabi **Using Guiding Heuristics to Improve the Dynamic Checking of Temporal Properties in Data Dominated High-Level Designs** Alair Dias Junior and Diogenes Silva Junior **Data Extraction from SystemC Designs using Debug Symbols and the SystemC API** Jannis Stoppe, Robert Wille and Rolf Drechsler
12:30-14:00	**Lunch break**	
14:00-15:00	**Invited talk: Manfred Glesner and François Philipp (TU Darmstadt)** **Embedded Systems Design for Smart System Integration**	
15:00-16:15	S3:Novel Processor Architectures **LImbiC: An Adaptable Architecture Description Language Model for Developing an Application-Specific Image Processor** Carsten Tradowsky, Tanja Harbaum, Shaver Deyerle and Juergen Becker **A reconfigurable multi-standard ASIP-based turbo decoder for an efficient dynamic reconfiguration in a multi-ASIP context** Vianney Lapotre, Purushotham Murugappa, Guy Gogniat, Amer Baghdadi, Michael Huebner and Jean-Philippe Diguet **A study on Polymorphing Superscalar Processor Dynamically to Improve Power Efficiency** Sudarshan Srinivasan, Rance Rodrigues, Arunachalam Annamalai, Israel Koren and Sandip Kundu	S4: Memory Design **Ground Gated 8T SRAM Cells with Enhanced Read and Hold Data Stability** Hailong Jiao and Volkan Kursun **A Discussion on SRAM Forward/Inverse Problem Analyses for RTN Long-Tail Distributions** Worawit Sohma, Hiroyuki Yamauchi and Ma Yuyu **Characterization of a Low Leakage Current and High-Speed 7T SRAM Circuit with Wide Voltage Margins** Khawar Sarfraz and Volkan Kursun
16:15-16:30	**Coffee break**	
16:30-17:45	S5: Security **Dynamic Encryption Key Design and Management for Memory Data Encryption in Embedded Systems** Mei Hong, Hui Guo and Sri Parameswaran **A Double-width Algorithmic Balancing to prevent Power Analysis Side Channel Attacks in AES** Ankita Arora, Jude Angelo Ambrose and Sridevan Parameswaran **State Encodings and Structural Modifications for Security: Methods for Reducing Peak Current Variations** Mike Borowczak and Ranga Vemuri	S6: CAD Tools and Methods **Simultaneous Gate Sizing and Vth Assignment using Lagrangian Relaxation and Delay Sensitivities** Guilherme Flach, Tiago J. Reimann, Gracieli Posser, Marcelo Johann and Ricardo Reis **STAIRoute: Global Routing using Monotone Staircase Channels** Bapi Kar, Susmita Sur-Kolay and Chittaranjan Mandal **A novel tool flow for increased routing configuration similarity in multi-mode circuits** Brahim Al Farisi, Elias Vansteenkiste, Karel Bruneel and Dirk Stroobandt
17:45-19:00	**Steering Comittee Meeting**	
19:00-20:00	**Welcome cocktail**	

Tuesday, August 6

09:00-10:00 — **Keynote 2: Erik Jan Marinissen (IMEC)**
Murphy Goes 3D

10:00-10:20 — **Coffee break**

10:20-12:00

S7: Reliability and Variability Issues

On-chip clock error characterization for clock distribution system
Chuan Shan, Dimitri Galayko and François Ançeau

Using Electromagnetic Emanations for Variability Characterization in Flash-Based FPGAs
Jimmy Fernando Tarrillo, Jorge Tonfat, Ricardo Reis, Fernanda Kastensmidt, Florent Bruguier, Morgan Bourrée, Pascal Benoit and Lionel Torres

Whitespace-Aware TSV Arrangement in 3D Clock Tree Synthesis
Xin Li, Wulong Liu, Haixiao Du, Yu Wang, Yuchun Ma and Huazhong Yang

Mitigate TSV Electromigration for 3D ICs - From the Architecture Perspective
Yuanqing Cheng, Aida Todri-Sanial, Alberto Bosio, Luigi Dilillo, Patrick Girard, Arnaud Virazel, Pascal Vivet and Marc Belleville

S8: Energy-aware Design Techniques

Program Phase Duration Prediction and its Application to Fine-Grain Power Management
Sudarshan Srinivasan, Raghavan Kumar and Sandip Kundu

Exploiting Body Biasing For Leakage Reduction: A Case Study
Andrea Manuzzato, Fabio Campi, Davide Rossi, Valentino Liberali and Davide Pandini

A power gating design framework integrated in a cycle accurate simulator
Davide Zoni and William Fornaciari

Saliency-driven Dynamic Configuration of HMAX for Energy-efficient Multi-object Recognition
Sungho Park, Ahmed Al Maashri, Yang Xiao, Kevin Irick and Vijaykrishnan Narayanan

12:00-14:00 — **Lunch break**

14:00-15:00 — **Invited talk: Lech Jozwiak (Technical Uiversity of Eindhoven)**
HW/SW Architecture Co-synthesis of ASIP-based MPSoCs for Highly-demanding Applications

15:00-16:15

Poster Intro

An Analytical Dynamic and Leakage Power Model for FPGAs
Hossein Mehri and Bijan Alizadeh

Symbolic Verification of Timed Asynchronous Hardware Protocols
Krishnaji Desai, Kenneth Stevens and John O'Leary

Distributed Resource Management in NoC-Based MPSoCs with Dynamic Cluster Sizes
Guilherme Machado de Castilhos, Marcelo Mandelli, Guilherme Madalozzo and Fernando Moraes

On Analyzing and Mitigating SRAM BER due to Random Thermal Noise
Vikram Suresh and Sandip Kundu

Power and Performance Evaluation of 3-D Stacked Floating-point Multipliers
Jubee Tada, Ryusuke Egawa and Hiroaki Kobayashi

Design of Reversible Decimal Compressors
Sai Phaneendra P, Chetan Vudadha, Sreehari Veeramachaneni, Syed Ershad Ahmed and Srinivas M B

Efficient use of solar power in micro scale solar energy harvesting through battery management
Hafeez Kt, Ghanashyam Hs, Ashudeb Dutta, Shiv Govind Singh and Shiva Kumar K

Routing-Aware Resource Allocation for Mixture Preparation in Digital Microfluidic Biochips
Sudip Roy, Partha P. Chakrabarti, Srijan Kumar, Bhargab B. Bhattacharya and Krishnendu Chakrabarty

On Run-time Task Graph Extraction in MPSoC
Kunal Ganeshpure and Sandip Kundu

High and Low Side High Voltage Switch with over current and over voltage protection
Walter Luis Tercariol, Richard Saez and Ivan Nascimento

A Novel Optimization Method for Reversible Logic Circuit Minimization
Matthew Morrison and Nagarajan Ranganathan

Neutron-induced Single Event Effects Analysis in a SAR-ADC Architecture Embedded in a Mixed-Signal SoC
Lucas Tambara, Fernanda Kastensmidt, Marcelo Lubaszewski, Tiago Balen and Paolo Rech

Behavioral Model of Integrated Qubit Gates for Quantum Reversible Logic Design
Matthew Lewandowski, Nagarajan Ranganathan and Matthew Morrison

Performance and Energy Efficient Cache System Design: Simultaneous Execution of Multiple Applications on Heterogeneous Cores
Venkateswaran Nagarajan, Akash Sridhar, Kartik Lakshminarasimhan, Prashanth Thinakaran, Rajagopal Hariharan, Vinesh Srinivasan, Ram Srivatsa Kannan and Aswin Kumar Sridharan

Comparison Between Three RTL and Standard Cells Models of the Multiplicative Inverse Calculation of Galois Field Elements for VLSI
Otacílio De Araœjo Ramos Neto, Antonio Carlos Cavalcanti and Ruy Alberto Pisani Altafim

16:15-16:30 — **Coffee break**

16:30-17:30 — **Poster Session**

17:30-18:00 — **CI Brazil Program**

18:00-19:30

19:30-22:30 — **Social Event**

Fogo & Chama Steak House

Wednesday, August 7	
09:00-10:00	**Keynote 3: Mircea Stan (University of Virginia)** **Breaking power delivery walls using voltage stacking**
10:00-10:20	**Coffee break**
10:20-11:20	Ph.D. Forum **Memory Subsystem Architecture Design for Multimedia Applications** Alexsandro Cristovao Bonatto and Altamiro Susin **Design & Implementation of Software Defined Radios on a Homogeneous Multi-Processor Architecture** Roberto Airoldi and Jari Nurmi **Design of Standard-Cell Libraries for Asynchronous Circuits with the ASCEnD Flow**Matheus Moreira and Ney L. V. Calazans **NoC Design and Optimization of Multicore Media Processors** Basavaraj Talwar and Bharadwaj Amrutur **Fault Recovery Communication Protocol for NoC-based MPSoCs** Eduardo Wächter, Alexandre Amory and Fernando Moraes **A Yield-driven Regular Layout Synthesis** Cristina Meinhardt and Ricardo Reis
11:20-12:00	
12:00-14:00	**Lunch break**
14:00-15:00	**Invited talk: Marcelo Johann (Universidade Federal do Rio Grande do Sul)** **Recent Advances and Challenges in Physical Design Automation**
15:00-16:15	S9:Logic and High Level Synthesis **Branch-and-Bound Style Resource Constrained Scheduling using Efficient Structure-Aware Pruning** Mingsong Chen, Saijie Huang, Geguang Pu and Prabhat Mishra **Logic Synthesis for Manufacturability Considering Regularity and Lithography Printability** Lucas Machado, Vinícius Dal Bem, Renato Ribas and André Reis **Iterative Remapping Respecting Timing Constraints** Lucas Machado, Vinicius Callegaro, Mayler Martins, Renato Ribas and André Reis
16:15-16:40	Closing session