SBCCI2009

TECHNICAL PROGRAM

Plenaries and Tutorials

Monday 09h00 – 10h30 (Room Cedro 5)

Michel M. Maharbiz - University of California Berkeley

TUTORIAL: A Cyborg Beetle: Wireless Neuronal Flight Control of a Free-flying Insect

Monday 11h00 – 12h30 (Room Cedro 5)

Mohamad Sawan - École Polytecnique Montréal

TUTORIAL: Emerging CMOS-Based biosensing technologies

Monday 14h00 – 15h30 (Room Cedro 5)

Calvin Plett - Carleton University

TUTORIAL: Design of Radio Frequency Components for Low-Power Short-Range Communications Systems

Monday 16h00 – 17h30 (Room Cedro 5)

André Inácio Reis - Instituto de Informática – UFRGS

TUTORIAL: "What about the IP of your IP?: An introduction to intelectual property law for engineers and scientists"

Tuesday 08h30 – 09h00 (Room Cedro 2)

Michel M. Maharbiz - University of California Berkeley

INVITED TALK: Building Micro-interfaces to Multicellular Systems: from Cyborg Insects to Synthetic Biology

Tuesday 14h00 – 14h30 (Room Cedro 2)

Mohamad Sawan - École Polytecnique Montréal

INVITED TALK: Multichannel neurorecording from the cortex: integration and packaging challenges

Tuesday 16h30 – 17h00 (Room Cedro 2)

Calvin Plett - Carleton University

INVITED TALK: Low-Power CMOS Transceiver with On-Chip Antenna for Short-Range Radio-Frequency Communicatio

SESSION 1 (Tuesday 9h00 – 10h30, Room Cedro 2): Embedded Systems

Chair: Edna Barros, UFPE

Low-power inter-core communication through cache configurability in embedded multiprocessors
Chenjie Yu and Peter Petrov

Exploiting the Model Driven Engineering Approach to Improve Design Space Exploration of Embedded System
Marcio F. da S. Oliveira, Ronaldo Rodrigues Ferreira, Francisco Assis do Nascimento, Franz Josef Rammig and Flavio Rech Wagner

A Hybrid Methodology for Tuning Two-Level Cache Hierarchy considering Energy and Performance
Abel Silva-Filho and Cristiano Araújo

Design of an Embedded System for the Proactive Maintenance of Electrical Valves
Luiz Fernando Gonçalves, Jefferson Luiz Bosa, Renato Ventura Bayan Henriques and Marcelo Lubaszewski

SESSION 2 (Tuesday 11h00 – 12h30, Room Cedro 2): Analog Design (1)

Chair: Wilhelmus Van Noije, USP

Determination of Distortion in Analog Multiplier Circuits by Two-Dimensional Integral Nonlinear Function
Luciano Abreu de Lacerda, Edson Pinto Santana, Cleber Vinicius Ribeiro de Almeida and Ana Isabela Araújo Cunha

A Fast-Response Charge-Pump Gate Driver Applied to Linear Regulation
Andre Mansano, Jader A. De Lima and Jacobus Swart

A self-protected integrated switch in a HV technology
Matias Miguez, Alfredo Arnaud and Joel Gak

SESSION 3 (Tuesday 14h30 – 16h00, Room Cedro 2): DSP and Arithmetic Circuits (1)

Chair: Volnei A. Pedroni, UTFPR

High Performance Motion Estimation Architecture Using Efficient Adder-Compressors.
André Silva, Marcelo Porto, Eduardo Costa and Sergio Bampi

Design of a Low Power MPEG-1 Motion Vector Reconstructor
Marco A. Ochoa-Montiel, Bashir M. Al-Hashimi and Peter Kollig

Dedicated Architecture for the Transforms and Quantization Loop of the H.264/AVC Intra Prediction
Robson Dornelles, Felipe Sampaio, Daniel Palomino and Luciano Agostini

SESSION 4 (Tuesday 17h00 – 18h30, Room Cedro 2): RF Design (1)

Chair: Fernando Rangel, UFRN

A Merged RF CMOS LNA-Mixer Design using Geometric Programming
Sergio Chaparro, Armando Ayala Pabón, Elkim Roa and Wilhelmus Van Noije

Phase noise - consumption trade-off in low power RF-LC-VCO design in micro and nanometric technologies
Rafaella Fiorelli and Fernando Silveira

A Novel Delta Sigma Built-In-Current-Sensor as a Signal Strength Indicator for RF Transceiver Reconfiguration
Laurent Leyssenne, Eric Kerhervé, Yann Deval and Didier Belot

SESSION 5 (Tuesday 16h30 – 18h00, Room Cedro 6): Test

Chair: Fernando Rangel, UFRN

A Parameter-Domain-based Methodology to Enhance Efficiency in Testbenches with Random Stimulation
Carlos Ivan Castro Marquez, Marius Strum and Wang Jiang Chau

Testing Configurable Quaternary Logic Blocks
Érika Cota, Luigi Carro, Felipe Pinto, Marcelo Lubaszewski and Ricardo Reis

A Logic Built-in Self-test architecture that reuses manufacturing compressed scan test patterns
Diogo Alves and Edna Barros

Simultaneous Impulse Stimulation and Response Sampling Technique for Built-In Self Test of On-Chip Linear Analog Circuits
Wimol San-um and Tachibana Masayoshi

SESSION 6 (Wednesday 08h30 – 10h00, Room Cedro 2): Network-on-Chip

Chair: Ricardo Jacobi, UnB

A Path-Load Based Adaptive Routing Algorithm for Networks-on-Chip
Leonel Tedesco, Fabien Clermidy and Fernando Moraes

Using NoC Routers as Processing Elements
Silvio Fernandes, Bruno Cruz and Ivan Saraiva

Adding Mechanisms for QoS to a Network-on-Chip.
Marcelo Daniel Berejuck and Cesar Albenes Zeferino

Improving Reliability in NoCs with Reconfigurable Router
Caroline Concatto, Debora Matos, Luigi Carro, Fernanda Kastensmidt, Marcio Kreutz and Altamiro Susin

SESSION 7 (Wednesday 08h30 – 10h30, Room Cedro 6): Analog Design (2)

Chair: Carlos Galup, UFSC

A Compact Low-Distortion Low-Power Instrumentation Amplifier
Jader A. De Lima

A Low-Voltage Bandgap Reference Source Based on the Current-Mode Technique
Juan José Carrillo, Elkim Roa, José Vieira and Wilhelmus Van Noije

Zero Quiescent Current Startup Circuit with Automatic Turning-off for Low Power Current and Voltage Reference
Alfredo Olmos, André Vilas Boas, Jefferson Soldera and André Mansano

Design of Multiple Output, Field Programmable CMOS Voltage Reference using Floating Gate Transistors

Arsh Josan, Karan Kumar and C.M. Markan

SESSION 8 (Wednesday 11h00 – 12h30, Room Cedro 2): Power Dissipation

Chair: Diogenes C. da Silva Jr.,UFMG

A High Abstraction, High Accuracy Power Estimation Model for Networks-on-Chip

Luciano Ost ,Guilherme Guindani, Leandro Soares Indrusiak ,CezarReinbrecht, Thiago Raupp, Fernando Moraes

DRAM Power Management and Energy Consumption: a Critical Assessment

Daniel Schmidt and Norbert Wehn

On the Energy-Efficiency of Software Transactional Memory

Felipe Klein, Alexandro Baldassin, Guido Araujo, Paulo Centoducatte and Rodolfo Azevedo

SESSION 9 (Wednesday 14h00 – 16h00, Room Cedro 2): Digital Design

Chair: Altamiro Susin, UFRGS

System concept for a FPGA based real-time capable automotive ECU restbus simulation system

Oliver Sander, Christoph Roth, Vitali Stuckert and Jürgen Becker

ASIC Design of a Novel High Performance Neuroprocessor Architecture for Multi Layered Perceptron Networks

Igor Dantas dos Santos Miranda

A Parametric Expression-Grain Reconfigurable Architecture

Juan eusse, Michael Hubner and Ricardo Jacobi

Improved Placement for Hierarchical FPGAs Exploiting Local Interconnect Resources

Valerij Matrose and Carsten Gremzow

SESSION 10 (Wednesday 14h00 – 15h30, Room Cedro 6): Sensor Design

Chair: Marcelo Antonio Pavanello, FEI

Pipelined Successive Approximation Conversion (PSAC) with Error Correction for a CMOS Ophthalmic Sensor
Frank Sill and Davies William de Lima Monteiro

Floating Gate MOSFET Circuit Design for its use in a Monolithic MEMS Gas Sensor.
Mario Alfredo Reyes-Barranca, Salvador Mendoza-Acevedo, Luis Martin Flores-Nava, Alejandro Avila-Garcia and Jose Luis Gonzalez-Vidal

SESSION 11 (Thursday 08h30 – 10h30, Room Cedro 2): DSP and Arithmetic Circuits (2)

Chair: Fernando Gehm Moraes, PUCRS

Parameterizable Floating-point Library for Arithmetic Operations in FPGAs
Diego F. Sanchez, Daniel M. Muñoz, Carlos H. Llanos and Mauricio Ayala-Rincón

High Throughput and Low Cost Architecture for H.264/AVC Context Adaptive Variable Length Decoder Targeting HDTV
Thaísa Silva, Fabio Pereira, Luciano Agostini, Altamiro Susin and Sergio Bampi

Architecture for Dense Matrix Multiplication on a High-Performance Reconfigurable System
Viviane Souza, Victor Medeiros, Derci Lima, Abner Barros, Paulo Sérgio Nascimento and Manoel Lima

Design of Low Complexity Digital FIR Filters
Levent Aksoy, Diego Jaccottet and Eduardo Costa

SESSION 12 (Thursday 14h00 – 16h00, Room Cedro 2): RF Design (2)

Chair: Calvin Plett, Carleton University

Voltage Controlled Delay Line With Phase Quadrature Outputs For [0.9-4] GHZ F-Dll Dedicated To Zero-If Multi-Standard Lo

Cedric Majek, Yann Deval, Hervé Lapuyade and Jean-Baptiste Bégueret

High IIP2 down-converter for homdyne receivers
Antônio Felipe Silva and Fernando Rangel de Sousa

Aspects Of Cross Inductor On 0.35µm CMOS Techonology
Luiz Carlos Moreira, Wilhelmus A. M. Van Noije, Armando Ayala Pabón and Andrés Farfán-Peláez

CMOS 2.45GHz RF Power Amplifier for RFID Reader
Md. Jasim Uddin, Mamun Bin Ibne Reaz, Muhammad Ibn Ibrahimy, Anis Nurashikin Nordin, Muhammad Asraful Hasan and Mohd Alauddin Mohd Ali

SESSION 13 (Thursday 14h00 – 16h00, Room Cedro 6): Reliability

Chair: Sergio Bampi, UFRGS

Reliability Aware Yield Improvement Technique for Nanotechnology Based Circuits
Costas Argyrides, Carlos Lisboa and Luigi Carro

Protecting Digital Circuits Against Hold Time Violation Due to Process Variability
Gustavo Neuberger, Gilson Wirth and Ricardo Reis

Twin Gates – Improved Reliability concerning Gate Oxide Breakdown by Redundancy
Hagen Saemrow, Claas Cornelius, Frank Sill, Andreas Tockhorn and Dirk Timmermann

SESSION 14 (Thursday 16h30 – 18h30, Room Cedro 2): Verification

Chair: Carlos Arthur Lang Lisbôa, UFRGS

A MDE Approach to the Formal Verification of UML based Embedded Systems Specifications
Francisco Assis Moreira Nascimento, Marcio Ferreira da Silva Oliveira and Flávio Rech Wagner

Function Verification of Power Gate Design in SystemC RTL