

Self-Consistent Simulation of Heating Effects in Nanoscale Devices

Dragica Vasileska¹, Katerina Raleva² and Stephen M. Goodnick¹

¹Arizona State University, Tempe, AZ USA, ²FEIT ó Skopje, Republic Macedonia
(vasileska@asu.edu, stephen.goodnick@asu.edu, katerina.raleva@asu.edu)

In this talk we present state of the art modeling of coupled electron-phonon transport in nanoscale CMOS SOI devices, in order to elucidate from a microscopic standpoint the role of device dimensions, device technologies and various material strategies on self-heating in this technology.

We have developed an in-house simulator to examine heat transport in nanoscaling devices, in which ensemble Monte Carlo simulation is used to simulate non-stationary transport coupled with moment expansion equations for the acoustic and optical phonon modes of the system. The temperature maps of the acoustic and optical phonon temperatures for 20 to 100 nm gate-length devices are shown in Fig. 1. These demonstrate that in short gate length devices, due to the non-stationary nature of the carrier transport, energy is dissipated towards the drain end of the device, and the hot spot (region of maximum temperature) moves towards the drain contact, resulting in less phonon scattering in the channel, reducing self-heating effects.

We have investigated the degree of self-heating using Silicon on Diamond (SOD) technology rather than SOI, where there is reduced heat degradation and better spreading of the heat in the Diamond material, as shown in Fig. 2. Interestingly, even though AlN has smaller thermal conductivity than Diamond, the current degradation for an AlN buried insulator is slightly lower due to the fact that the dielectric constant of AlN is higher which leads to better capacitive coupling in the structure. In the case of Diamond or AlN as buried oxides it becomes important to model the underlying silicon substrate [1].

Heating effects are also not the major issue in dual gate devices in which, even though we have about 6% more current degradation, the drive current is 1.5-1.7 times higher so we can trade slightly higher heating for significantly more current drive.

We also demonstrate for FD SOI devices that the use of the full phonon dispersion does not affect the conclusions regarding heating effects in these device structures, so the use of the linear and constant dispersion relation for acoustic and optical phonons, respectively, is justified.

It is important to note that tools for the thermal modeling of nanoscale devices need to be improved from the present state of the art as 3D tools are needed, for example, to simulate heat transport and electrical transport in a FinFET device. We will discuss preliminary results of such 3D model as well. The ultimate goal is to design the tool that can be efficient enough but at the same time can simulate most accurately both electrons and phonons within the particle pictures by solving their corresponding Boltzmann transport equations self-consistently.