SFORUM2009

TECHNICAL PROGRAM

SESSION 1 (Tuesday 9h00 – 10h30, Room Cedro 5)

First and Second Order Substrate Bias Influence on FinFETs
Mr. Rudolf Bühler (unirbuhler@fei.edu.br)

IMPACT OF THE HALO REGION ON FLOATING BODY EFFECTS IN TRIPLE GATE FINFETS
Milene Galeti (mgaleti@lsi.usp.br)

EVALUATION OF THE DRAIN LEAKAGE CURRENT BEHAVIOR IN DOUBLE GATE FINFETS
Mr. Jorge Giroldo Jr. (giroldo77@fei.edu.br)

CROSS-SECTION SHAPE INFLUENCE ON SURROUNDING MuGFETs
Mr. Marcelo Sandri (marcelo.sandri@gmail.com)

MULTIPLES THRESHOLD VOLTAGES IN TRAPEZOIDAL CHANNEL MUGFETS
Ms. Maria Glória Caño de Andrade (gloria@lsi.usp.br)

SESSION 2 (Tuesday 11h00 – 12h30, Room Cedro 5)

The Corner Effect Influence on Drain Current in Low-Dopped Rounded Corners Triple-Gate Devices
Mr. Rodrigo Bechelli (rprior@infranology.com.br)

SYSTEM TEST OF ELECTRON MULTIPLYING CCD CHARACTERIZATION
Mr. Julián David Rodríguez Ramirez (juliandavid1414@gmail.com)

TWO-DIMENSIONAL NUMERIC MODELING OF PLASMA ETCHING
Ms. Regina Peixoto (reginalira@gmail.com)

Control Access Using RFID Technology

Mr. Michael Taynnan (michael.taob@gmail.com)

ON THE ELMORE "FIDELITY" UNDER NANOSCALE TECHNOLOGIES
Mr. Tiago Reimann (tjreimann@inf.ufrgs.br)

SESSION 3 (Tuesday 9h00 – 10h30, Room Cedro 5)

IMPLEMENTATION OF RSA CRYPTOSYSTEM IMMUNE TO TIMING ATTACKS
Ms. Jamile Martins (p.jamile.eti@gmail.com)

FPGA DESIGN OF A MLP ARTIFICIAL NEURAL NETWORK ARCHITECTURE
Mr. Antonyus Ferreira (pyetrotype@gmail.com)

FPGA prototyping of an USB Host Controller
Mr. Hudson Veloso (huv@cin.ufpe.br)

A FPGA FFT CORE IMPLEMENTATION
Mr. Arthur Rolim (auar@cin.ufpe.br)

Functional Verification of a USB host controller.
Ms. Renata Garcia Oliveira (rgo@cin.ufpe.br)

ASPECTS OF IMPLEMENTATION OF AN EDUCATIONAL PLATFORM FOR ROBOTICS BASED FPGA
Mr. Felipe Gurgel (felipe-gurgel@hotmail.com)

TOWARDS ACCELERATING LOW-LEVEL VISION IN ROBOTICS
Mr. Gianna Araújo (gianna_araujo@yahoo.com.br)

SESSION 4 (Tuesday 11h00 – 12h30, Room Cedro 5)

AN ADDRESS DECODER FOR VARIABILITY CHARACTERIZATION FOR 65nm MOS TRANSISTORS.
Felipe Correa Werle (felipewerle@gmail.com)

LAYOUT DESIGN OF CMOS INVERTERS WITH CIRCULAR AND CONVENTIONAL GATE MOSFETs BY USING IC STATION OF MENTOR
Mr. Klaus Cirne (klauscirne@gmail.com)

IMPLEMENTING DIAMOND SOI MOSFET LAYOUT
Raffaello Claser (rclaser@globo.com)

MAPPING AND UNDERSTANDING THE MULTIVARIATE AND MULTI-OBJECTIVE OPTIMIZATION BEHAVIOUR OF A SOI CMOS OTA USING GENETIC ALGORITHMS
Mr. Thiago Turcato do Rego

PLANAR TRANSISTOR NETWORK VISUALIZATION ALGORITHM
Mr. Rafael Hansen da Silva (rhsilva@inf.ufrgs.br)

SESSION 5 (Wednesday 08h30 – 10h00, Room Cedro 5)

A PHASE AND FREQUENCY DETECTOR AND CHARGE PUMP FOR LOCAL OSCILLATOR IN A ZIGBEE TRANSCEIVER
Mr. Guilherme Freitas (gmfreitas@inf.ufrgs.br)

DESIGN AND CHARACTERIZATION OF A 900MHZ LC VOLTAGE CONTROLLED CMOS OSCILLATOR
Mr. Heider Marconi Guedes Madureira (heider.marconi@gmail.com)

A NEW LOW POWER EXPLORATION MECHANISM BASED ON DESIGN OF EXPERIMENTS (DOE) AND TWO-LEVEL HIERARCHIES
Prof. Filipe Rolim Cordeiro (frc@cin.ufpe.br)

DESIGN OF AN ANALOG-TO-DIGITAL CONVERTER
Mr. Leandro Mota (leandromota.rn@gmail.com)

Impact of Different OP-AMPs in CMOS Bandgap References Implemented In 018um Technology
Mr. Dalton Colombo (dmcolombo@inf.ufrgs.br)

SESSION 6 (Wednesday 11h00 – 12h30, Room Cedro 5)

WIRELESS TEMPERATURE SENSING USING ZIGBEE NETWORKS
Mr. Marcelo Besch

An UDP/IP network stack in FPGA
Mr. Fernando Luís Herrmann (herrmann@mail.ufsm.br)

REDUCING SOC DESIGN EFFORT BY ABSTRACTING COMMUNICATION DETAILS USING A ESL CENTRIC SERVICE BASED UML PROFILE
Ms. Millena Gomes (maag@cin.ufpe.br)

A FPGA{-}based Network stack with a reduced number of layers
Mr. Josue P. J. de Freitas (josue.freitas@gmail.com)

NETWORK-ON-CHIP PERFORMANCE EVALUATION ON FPGA: A HARDWARE/SOFTWARE CORE-BASED SOLUTION
Mr. Miklécio Costa (miklecio.costa@inf.ufrgs.br)

SESSION 7 (Wednesday 14h00 – 15h30, Room Cedro 5)

ANALYSIS OF POWER CONSUMPTION USING A NEW METHODOLOGY FOR THE CAPACITANCE MODELING OF COMPLEX LOGIC GATES WITH DOGBONE TRANSISTOR
Mr. Sidinei Ghissoni (sghissoni@inf.ufrgs.br)

EVALUATION OF STANDARD CELL LIBRARIES WITH DIFFERENT TEMPLATES AND GATE DESIGN APPROACHES
Mr. Diogo da Silva (dcsilva@inf.ufrgs.br)

EFFECT OF COMPLEX CELL FUNCTIONS IN THE TECHNOLOGY MAPPING PROCESS
Mr. Pedro Egidio Menegaz Paganela (pempaganela@gmail.com)

A KERNEL-BASED APPROACH FOR FACTORING LOGIC FUNCTIONS
Mr. Vinicius Callegaro (vcallegaro@inf.ufrgs.br)

SESSION 9 (Thursday 14h00 – 16h00, Room Cedro 5)

CMOS A/D FLASH CONVERTER BASED ON THE QUANTIZATION OF THE THRESHOLD VOLTAGE
Mr. André Dantas Ferreira

AN OPTIMIZATION-BASED TOOL FOR CIRCUIT LEVEL SYNTHESIS ANALOG INTEGRATED CIRCUITS
Lucas Compassi Severo (lucascs.eletrica@gmail.com)

VHDL-AMS Modeling of Analog/Mixed-Signal IP Blocks
Mr. Joao Vitor Pimentel (jv.bernatel@gmail.com)

MEASUREMENT RESULTS OF THE UFRN DIDACTIC CHIP
Mr. Francisco Júnior (fmarcelinobjr@gmail.com)

2-INPUT NEUROMORPH/IC AND LOGIC GATE BASED ON INTEGRATE-AND-FIRE NEURON USING CMOS TECHNOLOGY
Mr. Leonardo Enzo Brito da Silva (leonardoenzob@gmail.com)

SESSION 10 (Thursday 16h30 – 18h30, Room Cedro 5)

Implementing a Multichannel High Speed DDR SDRAM Memory Controller: A Study Case for H.264 Decoder
Mr. Alexsandro Bonatto (bonatto@eletro.ufrgs.br)

An H.264/AVC Decoder Frontend Targeting Broadcasting DTV for SBTVD
Mr. Márlon Lorencetti (marlonlorencetti@gmail.com)

A NETWORK-ON-CHIP BASED ARCHITECTURE FOR H.264 MOTION ESTIMATION
Ms. Alba Sandyra Bezerra Lopes (alba@lasic.ufrn.br)

The importance of establishing a methodology for analysis of an algorithm between architectures
Mr. BRUNO SILVA (bcs2@cin.ufpe.br)

CABARE: AN EDUCATIONAL RECONFIGURABLE GENERAL PURPOSE PROCESSOR
Mr. Tadeu Ferreira Oliveira (tadeu@lasic.ufrn.br)